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PLANTRONICS, INC. 345 ENCINAL STREET P.O. BOX 635 SANTA CRUZ, CA 95060-0635			EXAMINER RYMAN, DANIEL J	
			ART UNIT 2665	PAPER NUMBER

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/401,070

Applicant(s)

ANDERSON ET AL.

Examiner

Daniel J. Ryman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-54 and 56-79 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-54 and 56-79 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Amendment*

1. Examiner acknowledges the filing of an RCE on 5/23/2005.
2. Applicant's arguments with respect to claims 15-39, 51-54, and 56-69 have been considered but are moot in view of the new ground(s) of rejection.
3. Applicant's arguments filed 5/23/2005 have been fully considered but they are not persuasive. On pages 17-19 of the Response, regarding claims 1-14, Applicant asserts that "Endick neither discloses nor suggests that a headset adapter independently and directly controls the headset accessory." However, Examiner submits that, as currently worded, the claims do not require the headset adapter to independently and directly control the headset accessory. In claim 1, the pertinent limitation contains the wording "accessory can be independently and directly controlled." The phrase "can be" does not require the accessory to be independently and directly controlled. Rather the phrase "can be" only requires that the accessory have the capability of being independently and directly controlled. Even if Endick does not disclose that the accessory is independently and directly controlled, Endick nonetheless discloses an accessory that *can be* independently and directly controlled. Therefore Applicant argues that claims 1-14 are patentable over the cited prior art based on a limitation that does not effectively limit the scope of the claims. As such, Examiner maintains that claims 1-14 are obvious given the cited prior art.
4. On pages 17-19 of the Response, regarding claims 26-39, Applicant asserts that "Endick neither discloses nor suggests that a headset adapter independently and directly controls the headset accessory." However, Examiner submits that, as currently worded, the claims do not require the headset adapter to independently and directly control the headset accessory. Claims

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26 and 33 claim an interface bus and an intended use for the bus, namely that the bus is used as a conduit for transport of control and monitoring information. According to MPEP § 2106(II)(C), “[l]anguage that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure” includes “statements of intended use of field of use.” Such language “does not limit the scope of a claim or claim limitation.” Therefore Applicant argues that claims 26-39 are patentable over the cited prior art based on a limitation that does not limit the scope of the claims. As such, Examiner maintains that claims 26-39 are obvious given the cited prior art.

5. On pages 17-19 of the Response, regarding claims 40-50 and 70-79, Applicant asserts that “Endick neither discloses nor suggests that a headset adapter independently and directly controls the headset accessory.” However, Examiner submits that, as currently worded, the claims do not require the headset adapter to independently and directly control the headset accessory. Claims 40, 70, and 75 contains the limitation “transmitting a command or status request signal from the headset adapter base . . . in order for the headset adapter base to independently and directly control and monitor operation of the accessory,” or a similar limitation, where the “in order . . .” language is an intended use. According to MPEP § 2106(II)(C), “[l]anguage that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure” includes “statements of intended use of field of use.” Such language “does not limit the scope of a claim or claim limitation.” Therefore Applicant argues that claims 40-50 and 70-79 are patentable over the cited prior art based on a limitation that does not limit the scope of the claims. As such, Examiner maintains that claims 40-50 and 70-79 are obvious given the cited prior art.

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6. On pages 17-19 of the Response, regarding claims 51-54, Applicant asserts that "Endick neither discloses nor suggests that a headset adapter independently and directly controls the headset accessory." However, Examiner submits that, as currently worded, the claims do not require the headset adapter to independently and directly control the headset accessory. Claim 51 contains the limitation "[a] data packet transmitted over an accessory interface bus . . . thereto for directly and independently controlling, monitoring and testing," where the "thereto for . . ." language is an intended use. According to MPEP § 2106(II)(C), "[l]anguage that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure" includes "statements of intended use of field of use." Such language "does not limit the scope of a claim or claim limitation." Therefore Applicant argues that claims 51-54 are patentable over the cited prior art based on a limitation that does not limit the scope of the claims. As such, Examiner maintains that claims 51-54 are obvious given the cited prior art.

7. Given the above arguments, Examiner maintains that claims 1-14, 26-50, and 70-79 are obvious given the cited prior art. Claims 15-39, 51-54, and 56-69 have been rejected using a new grounds of rejection. The rejections follow.

***Claim Rejections - 35 USC § 112***

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 15-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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10. Claim 15 discloses “at least one accessory to the telecommunications headset which is coupled to the interface bus.” In this limitation, it is unclear whether the phrase “which is coupled to the interface bus” modified the headset or the accessory. Possible changes to this limitation include: “at least one telecommunications headset accessory which is coupled to the interface bus” and “at least one accessory to the telecommunications headset wherein the headset is coupled to the interface bus”.

11. Claim 26 discloses “A telephone headset accessories interface bus for controlling and monitoring a telephone headset accessory.” Examiner submits that the bus neither controls nor monitors the accessory, but rather the bus simply carries packets that have been transmitted by and will be received by devices connected to the bus. Therefore, “A telephone headset accessories interface bus for controlling and monitoring a telephone headset accessory” should be “A telephone headset accessories interface bus for carrying control and monitoring information destined for a telephone headset accessory”.

12. Claim 33 discloses “An interface bus that transmits and receives a plurality of communication packets between a headset adapter and a headset accessory.” Examiner submits that the bus neither transmits nor receives packets, but rather the bus carries packets that have been transmitted by and will be received by devices connected to the bus. Therefore, “An interface bus that transmits and receives a plurality of communication packets between a headset adapter and a headset accessory” should be “An interface bus that carries a plurality of communication packets between a headset adapter and a headset accessory”.

***Claim Rejections - 35 USC § 101***

13. 35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

14. Claims 56-62 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 56-62 are directed to a communications protocol comprising a plurality of commands. However, the communications protocol is not implemented by any mechanism. As such, the communications protocol is merely functional descriptive material rather than statutory subject matter.

15. Claims 63-65 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 63-65 are directed to a combination of an interface bus and a protocol. However, the communications protocol is not implemented by any mechanism. As such, the communications protocol is merely functional descriptive material rather than statutory subject matter.

16. Claims 66-69 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 66-69 are directed to a combination of a headset adapter and a protocol. However, the communications protocol is not implemented by any mechanism. As such, the communications protocol is merely functional descriptive material rather than statutory subject matter.

***Claim Rejections - 35 USC § 103***

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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18. Claim 1-3, 14, 26, 27, 33, 40, 45, 70, 71, 75, and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art.

19. Regarding claims 1, 14, 26, 33, 70, and 75, Endick discloses a telecommunication system comprising: a telephone handset (ref. 106 and col. 3, lines 4-13); an accessory adapter (option bus and microcontroller) coupled to the telephone handset and having an accessory interface bus (option bus) for transmitting and receiving communications packets, the adapter being configured to be coupled to a base telephone (Figs. 1, 4, and 5; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38) where the accessories include a headset attachment (col. 3, lines 66-68); a micro-controller coupled to the interface bus (ref. 118; col. 3, lines 27-36; and col. 5, lines 22-42), for controlling and monitoring at least one accessory to the telecommunications headset which is coupled to the interface bus (col. 3, lines 27-36 and col. 5, lines 22-42), wherein the micro-controller controls and monitors the accessory through the bi-directional transmission of communications packets between the micro-controller and the accessory via the interface bus (col. 3, lines 27-36 and col. 5, lines 22-42) with one purpose being to test the accessory and verify proper operation of the accessory (col. 8, lines 7-10); and an accessory for the telephone coupled to the accessory interface bus of the headset adapter, wherein the accessory can be directly controlled and monitored by the headset adapter independently of the base telephone via the transmission of communications packets between the accessory and the headset adapter over the accessory interface bus (col. 3, lines 4-14; col. 3, line 27-36; col. 3, line 58-col. 4, line 10; col. 5, lines 22-42; col. 6, lines 47-64; col. 8, lines 15-29; and col. 9, lines 1-6) where "can be" only requires that the accessory have the capability of being directly controlled and monitored.



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Endick does not disclose that the telecommunication system comprises a telephone headset and a headset adapter coupled to the telephone headset and having an accessory interface bus. However, Endick does disclose having an accessory interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). This bus is part of an accessory adapter where the accessory adapter is broadly defined to be a system which interfaces a phone system to accessories. Endick also discloses that these accessories can include a telephone headset (col. 3, lines 66-68). It would have been obvious to one of ordinary skill in the art to have the telecommunication system comprise a telephone headset and a headset adapter where the headset adapter is broadly defined to be the accessory adapter since it is known in the art to include a telephone headset as an accessory item in order to allow a user of the telecommunication system to use the headset.

Additionally, Endick does not expressly disclose that the accessories are headset accessories since Endick only expressly discloses accessories for the base telephone. However, Endick does leave open the possibility for the accessories to be headset accessories by disclosing that the accessories are not limited to the aforementioned accessories for the base telephone (col. 3, line 66-col. 4, line 2). Applicant admits that accessories for a telephone headset are well known as prior art (page 1, line 13-page 2, line 21) where the accessories are used to add functionality to or ease the use of a telephone headset. It is also very old and well known in the art to use buses to communicate between devices connected to the bus, and thus it would have been obvious to one of ordinary skill in the art at the time of the invention that the bus could be used to add accessories to another accessory. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the accessories include accessories for the telephone

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headset since accessories to telephone headsets are very well known as a means to add functionality to or ease the use of a telephone headset.

20. Regarding claims 2, 71, and 76, Endick in view of Applicant's admitted prior art discloses that the accessory interface bus includes at least one bi-directional signaling line for transmitting and receiving the communications packets between the accessory and the headset adapter in order to control and monitor the accessory (col. 8, lines 15-29).

21. Regarding claims 3 and 27, Endick in view of Applicant's admitted prior art discloses that the accessory interface bus further includes: a power bus containing lines for +/- 5V and +/- VAUX (col. 3, lines 58-60 and col. 5, lines 43-48) where the +5V and +VAUX is broadly defined as a high voltage rail and the -5V and -VAUX is broadly defined as a low voltage rail; and at least one bi-directional signaling line for transmitting and receiving communications packets between the accessory and the headset adapter in order to control and monitor the accessory (col. 8, lines 15-29).

22. Regarding claim 40, Endick discloses a method for controlling or monitoring an accessory to a telephone using an accessory adapter base and an interface bus, the method comprising: detecting whether an accessory is coupled to the interface bus (polling) (col. 8, lines 15-29); and transmitting a command or status request signal from the headset adapter base over the interface bus and to the accessory, the headset adapter base being configured to be connected to a base telephone (col. 6, lines 47-64 and col. 8, line 15-col. 9, line 36). Here the "in order for" clause of the claim is an intended use which does not limit the scope of the claim and therefore is not part of the rejection.

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Endick does not disclose that the telecommunication system comprises a telephone headset and a headset adapter coupled to the telephone headset and having an accessory interface bus. However, Endick does disclose having an accessory interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). This bus is part of an accessory adapter where the accessory adapter is broadly defined to be a system which interfaces a phone system to accessories. Endick also discloses that these accessories can include a telephone headset (col. 3, lines 66-68). It would have been obvious to one of ordinary skill in the art to have the telecommunication system comprise a telephone headset and a headset adapter where the headset adapter is broadly defined to be the accessory adapter since it is known in the art to include a telephone headset as an accessory item in order to allow a user of the telecommunication system to use the headset.

Additionally, Endick does not expressly disclose that the accessories are headset accessories since Endick only expressly discloses accessories for the base telephone. However, Endick does leave open the possibility for the accessories to be headset accessories by disclosing that the accessories are not limited to the aforementioned accessories for the base telephone (col. 3, line 66-col. 4, line 2). Applicant admits that accessories for a telephone headset are well known as prior art (page 1, line 13-page 2, line 21) where the accessories are used to add functionality to or ease the use of a telephone headset. It is also very old and well known in the art to use buses to communicate between devices connected to the bus, and thus it would have been obvious to one of ordinary skill in the art at the time of the invention that the bus could be used to add accessories to another accessory. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the accessories include accessories for the telephone

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headset since accessories to telephone headsets are very well known as a means to add functionality to or ease the use of a telephone headset.

23. Regarding claim 45, Endick in view of Applicant's admitted prior art discloses receiving a response signal from the accessory returning information on the current status of the accessory when a status request signal is transmitted (col. 8, line 15-col. 9, line 36).

24. Claims 4-6, 28, 29, 34, 35, 41, 46, 72-74, and 77-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art as applied to claims 1, 26, 33, 40, 45, 70, and 75 above, and further in view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488).

25. Regarding claims 4, 28, 34, 41, 46, 72, and 77, Endick in view of Applicant's admitted prior art does not expressly disclose that each communications packet includes a synch pulse which defines a transmission rate for the communications packet. Yamaguchi discloses, in a bi-directional communication system, having a synch pulse contained in each packet (col. 8, lines 10-15 where a frame and a packet can be viewed as being analogous). Yamaguchi further discloses that synch pulses are well known in the art (col. 10, lines 9-14). Typically a synch pulse is used in order to ensure that the transmitter and receiver have the same clock signal. If there is a mismatch in clocking, the receiver may not sample fast enough (sample for the wrong transmission rate) or it may sample at the wrong time periods such that the receiver will not be able to properly read a transmitted signal, as is evidenced by King (col. 2, lines 10-39). It is also obvious that such a system would allow for a variety of transmission rates to be used such that each accessory defines its own transmission rate using the synch pulse. It would have been obvious to one of ordinary skill in the art of packet communications to include a synch pulse

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which defines a transmission rate for the communications packet to ensure that the receiver will properly sample the incoming signal.

26. Regarding claims 5, 29, 35, 73, and 78, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King discloses that the synch pulse includes a bit having a bit period which defines the synchronization for the communications packet (King: col. 1, line 64-col. 2, line 39, esp. col. 2, lines 31-39). It is obvious that in order to achieve bit synchronization, the transmission rate needs to be determined so that the receiver will know when to expect the next bit and so when to sample the transmitted signal. Endick in view of Yamaguchi in further view of King implements synchronization with a rate bit in order to minimize the amount of hardware used to generate the transmitted signal (King: col. 1, line 64-col. 2, line 6). It would have been obvious to one of ordinary skill in the art of packet communications to have the synch pulse include a rate bit having a bit period which defines the transmission rate for the communication packet in order to minimize the amount of hardware used to generate the transmitted signal.

27. Regarding claims 6, 74, and 79, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King discloses that the rate bit includes a rising edge and a falling edge within the bit period (King: col. 2, lines 24-28) and that a duration of time between the rising edge and the falling edge is used to determine the bit period (King: col. 2, lines 24-28) where "equally spaced signal level transitions occur during each address bit period so as to thereby define a plurality of data bit periods in each address bit period" is taken to mean that the duration between a rising and falling edge (equally spaced signal level transitions) is used to determine a bit period (define a data bit period). Endick in view of Applicant's

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admitted prior art in further view of Yamaguchi in further view of King does not expressly state that the bit period is inversely related to the transmission rate of the communications packet; however, it is well known in the art that a bit period is defined to be the inverse of the transmission rate.

28. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art in further view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) as applied to claims 5 and 17 above, and further in view of Miesterfeld et al (USPN 4,706,082).

29. Regarding claim 7, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King does not disclose that the synch pulse holds the accessory bus at a predetermined level for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets. Miesterfeld discloses, in a system using a serial data bus, having in every packet start bits, which are used by a detector to determine if another transmitter has started to transmit almost simultaneously, so that collisions due to an almost simultaneous transmission are avoided (col. 5, lines 23-39). These start bits occur at the beginning of the message and it would be obvious to include the start bits in the synch pulse which also comes at the beginning of the message. Also because the start bits are used to indicate a beginning of a message and aid in determining if there is a collision, it would be obvious to locate the start bits before the rate bit, which is an important part of the message and so should be sent only after it is determined that the bus is clear. Thus it would have been obvious to one of ordinary skill in the art of communications to have the synch pulse hold the bus at a predetermined level (have start

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bits) for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets.

30. Regarding claim 8, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King in further view of Miesterfeld does not expressly disclose that the synch pulse holds the accessory interface bus to a low voltage value for at least two bit periods before the rate bit is transmitted in order to prevent collision between communications packets. However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The length of the duration and the value of the start bits are not critical to the operation of the disclosed system, and therefore it would be obvious to use any number of bit periods or any value.

31. Claims 9, 10, 30, 31, 36, 37, 43, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art as applied to claims 1, 26, 33, 40, and 45 above, and further in view of Waechter et al (USPN 4,943,963).

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32. Regarding claims 9, 30, 36, and 47, Endick in view of Applicant's admitted prior art discloses that a slave select line is used to address a packet to an accessory (col. 5, lines 33-35) and that each option contains an ID (address) (col. 8, lines 44-46). Endick in view of Applicant's admitted prior art does not disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet; however, using addresses to identify a source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art and would allow the elimination of slave select lines within Endick in view of Applicant's admitted prior art's system. In further regards to claim 30, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The length of the destination address is not deemed essential to the



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operation of the disclosed interface bus, and so it would be obvious to have the address be any length including a byte.

33. Regarding claims 10, 31, 37, and 43, Endick in view of Applicant's admitted prior art in further view of Waechter discloses that the communications packet further includes a checksum for detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

34. Claims 11-13, 32, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art as applied to claims 1, 26, and 33 above, and further in view of Jones et al (USPN 5,140,611).

35. Regarding claim 11, Endick in view of Applicant's admitted prior art discloses that each communications packet includes a plurality of bits with each bit in the plurality of bits having an assigned value of zero or one (col. 5, lines 22-25). Endick in view of Applicant's admitted prior art does not disclose that each bit includes a first signal portion having a first logic level and a second signal portion having a second logic level and the assigned value of zero or one is assigned to each bit based upon a duration of either the first signal portion or the second signal portion. Jones teaches, in a communication system, (Fig. 2; col. 2, lines 34-52; col. 2, lines 61-67; and col. 5, lines 36-44) in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each bit includes a first signal portion having a first logic level and a second signal portion having a second logic level and the assigned value of zero or one is assigned to each bit based upon a duration of either the first signal portion or the second signal portion in order to have a data stream which is self-clocking.

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36. Regarding claim 12, Endick in view of Applicant's admitted prior art in further view of Jones discloses that if the duration of the at least one portion falls within a first range the bit is assigned a value of zero and if the duration of the at least one portion falls within a second range, the bit is assigned a value of one (Jones: Fig. 2; col. 2, lines 34-52; col. 2, lines 61-67; and col. 5, lines 36-44).

37. Regarding claim 13, Endick in view of Applicant's admitted prior art in further view of Jones discloses that each bit in the plurality of bits has a rising edge and a falling edge, and the rising edge and the falling edge are used to synchronize transmission of the communications packet after each bit is transmitted (Jones: Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53).

38. Regarding claims 32 and 38, Endick in view of Applicant's admitted prior art does not expressly disclose that each communications packet includes a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted. Jones discloses, in a communication system, having each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted (Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53). Jones does this in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each

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communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted in order to have a data stream which is self-clocking.

39. Regarding claim 39, Endick in view of Applicant's admitted prior art in further view of Jones discloses that each bit in the plurality of bits has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge can be used to synchronize transmission of the communications packet after each bit period (Jones: Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53).

40. Claims 42, 44, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art in further view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) as applied to claims 41 and 46 above, and further in view of Waechter et al (USPN 4,943,963).

41. Regarding claim 42, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King discloses that a slave select line is used to address a packet to an accessory (Endick: col. 5, lines 33-35) and that each option contains an ID (address) (Endick: col. 8, lines 44-46) and communicating a slave address (Yamaguchi: col. 3, lines 32-35). Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King does not disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet; however, using addresses to identify a

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source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art.

42. Regarding claim 44, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King in further view of Waechter discloses that the communications packet further includes a checksum for detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

43. Regarding claim 48, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King does not expressly disclose that the communications packet further includes a checksum for detecting errors in transmission of the communications packet from the accessory to the adapter base; however, using a checksum to detect errors in a communications packet is well known in the art, as is evidenced by Waechter (col. 5, lines 25-45). It would have been obvious to one of ordinary skill in the art at the time of the invention to have a checksum in order to ensure that the packet was transmitted properly.

44. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art as applied to claim 40 above, and further in view of Miesterfeld et al (USPN 4,706,082).

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45. Regarding claim 49, Endick in view of Applicant's admitted prior art does not disclose that the synch pulse holds the accessory bus at a predetermined level for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets. Miesterfeld discloses, in a system using a serial data bus, having in every packet start bits, which are used by a detector to determine if another transmitter has started to transmit almost simultaneously, so that collisions due to an almost simultaneous transmission are avoided (col. 5, lines 23-39). These start bits occur at the beginning of the message and it would be obvious to include the start bits in the synch pulse which also comes at the beginning of the message. Also because the start bits are used to indicate a beginning of a message and aid in determining if there is a collision, it would be obvious to locate the start bits before the rate bit, which is an important part of the message and so should be sent only after it is determined that the bus is clear. Thus it would have been obvious to one of ordinary skill in the art of communications to have the synch pulse hold the bus at a predetermined level (have start bits) for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets.

46. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art in further view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) as applied to claim 41 above, and further in view of Jones et al (USPN 5,140,611).

47. Regarding claim 50, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King does not disclose that the communications packet includes a

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plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are be used to synchronize transmission of the command or status request signal after each bit is transmitted. Jones discloses, in a communication system, having each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted (Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53). Jones does this in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted in order to have a data stream which is self-clocking.

48. Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art in further view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) in further view of Waechter et al (USPN 4,943,963).

49. Regarding claim 51, Endick discloses a data packet transmitted over an accessory interface bus having a number of devices coupled thereto (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; col. 6, lines 47-64; and col. 4, lines 20-38). Here the "thereto for" clause of the

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claim is an intended use which does not limit the scope of the claim and therefore is not part of the rejection.

Endick does not disclose that the telecommunication system comprises a telephone headset and a headset adapter coupled to the telephone headset and having an accessory interface bus. However, Endick does disclose having an accessory interface bus (Fig. 4; col. 3, lines 4-14; col. 3, line 58-col. 4, line 10; and col. 4, lines 20-38). This bus is part of an accessory adapter where the accessory adapter is broadly defined to be a system which interfaces a phone system to accessories. Endick also discloses that these accessories can include a telephone headset (col. 3, lines 66-68). It would have been obvious to one of ordinary skill in the art to have the telecommunication system comprise a telephone headset and a headset adapter where the headset adapter is broadly defined to be the accessory adapter since it is known in the art to include a telephone headset as an accessory item in order to allow a user of the telecommunication system to use the headset.

Additionally, Endick does not expressly disclose that the accessories are headset accessories since Endick only expressly discloses accessories for the base telephone. However, Endick does leave open the possibility for the accessories to be headset accessories by disclosing that the accessories are not limited to the aforementioned accessories for the base telephone (col. 3, line 66-col. 4, line 2). Applicant admits that accessories for a telephone headset are well known as prior art (page 1, line 13-page 2, line 21) where the accessories are used to add functionality to or ease the use of a telephone headset. It is also very old and well known in the art to use buses to communicate between devices connected to the bus, and thus it would have been obvious to one of ordinary skill in the art at the time of the invention that the bus could be

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used to add accessories to another accessory. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the accessories include accessories for the telephone headset since accessories to telephone headsets are very well known as a means to add functionality to or ease the use of a telephone headset.

Endick in view of Applicant's admitted prior art does not disclose that the data packet comprises: a synch pulse having a rate bit that defines a rate at which the data packet is being transmitted. Yamaguchi discloses, in a bi-directional communication system, having a synch pulse contained in each packet (col. 8, lines 10-15 where a frame and a packet can be viewed as being analogous. Yamaguchi further discloses that synch pulses are well known in the art (col. 10, lines 9-14). Typically a synch pulse is used in order to ensure that the transmitter and receiver have the same clock signal. If there is a mismatch in clocking, the receiver may not sample fast enough (sample for the wrong transmission rate) or it may sample at the wrong time periods such that the receiver will not be able to properly read a transmitted signal, as is evidenced by King (col. 2, lines 10-39). It is also obvious that such a system would allow for a variety of transmission rates to be used such that each accessory defines its own transmission rate using the synch pulse. It would have been obvious to one of ordinary skill in the art of packet communications to include a synch pulse which defines a transmission rate for the communications packet to ensure that the receiver will properly sample the incoming signal.

Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King does not disclose that the communication packet includes a source address indicating a bus address of the source of the communications packet and a destination address indicating a bus address of the destination of the communications packet. Endick in view of



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Applicant's admitted prior art in further view of Yamaguchi in further view of King discloses that a slave select line is used to address a packet to an accessory (Endick: col. 5, lines 33-35) and that each option contains an ID (address) (Endick: col. 8, lines 44-46) and communicating a slave address (Yamaguchi: col. 3, lines 32-35). However, using addresses to identify a source and a destination is well known in the art. For instance, Waechter discloses, in a bi-directional bus communication system, the use of a source address for indicating the source of the packet and a destination address for indicating the destination of the packet (col. 5, lines 21-53). It would have been obvious to one of ordinary skill in the art of communications to include a destination address in order to indicate for which unit the packet is destined and a source address in order to indicate from which unit the packet originated since such addressing is well-known in the art.

50. Regarding claim 52, referring to claim 51, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King in further view of Waechter discloses that the communications packet further includes a checksum for detecting errors in the transmission of the communications packet (Waechter: col. 5, lines 25-45).

51. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endick et al (USPN 5,339,360) in view of Applicant's admitted prior art in further view of Yamaguchi (USPN 5,278,848) in further view of King (USPN 3,793,488) in further view of Waechter et al (USPN 4,943,963) as applied to claim 51 above, and further in view of Jones et al (USPN 5,140,611).

52. Regarding claims 53 and 54, referring to claim 51, Endick in view of Applicant's admitted prior art in further view of Yamaguchi in further view of King in further view of

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Waechter does not disclose that the communications packet includes a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are be used to synchronize transmission of the command or status request signal after each bit is transmitted. Jones discloses, in a communication system, having each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted (Fig. 2; col. 2, lines 34-52; col. 2, lines 53-67; and col. 5, lines 36-53). Jones does this in order to allow the stream of data to be self-clocking. It would have been obvious to one of ordinary skill in the art at the time of the invention to have each communications packet include a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted in order to have a data stream which is self-clocking.

*Allowable Subject Matter*

53. Claims 15-25 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. The prior art does not disclose or fairly suggest having the headset adapter base directly and independently control the accessories.

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***Conclusion***

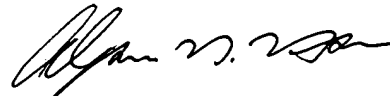
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 7:00-4:30 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*DJR*

Daniel J. Ryman  
Examiner  
Art Unit 2665



ALPUS H. HSU  
PRIMARY EXAMINER